

Development of a Single-Switch Quasi-Resonant High Voltage Gain DC–DC Converter with Coupled Inductor

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ABSTRACT: Renewable sources of energy are increasingly valued worldwide because of energy shortage and environmental contamination. Renewable energy systems such as Fuel cells, Wind power generation systems and photovoltaic systems generate low output voltage so it cannot be directly connected with grid. While connecting these renewable energy systems directly with grid leads to voltage mismatching problems. So the output voltage of renewable energy systems must be stepped up in order to connect it with grid. A novel multilevel DC-DC Boost converter is proposed to avoid voltage mismatching problems between low voltage photovoltaic arrays and the required higher voltage of the grid. The proposed converter consists of only one inductor, $(m-1)$ capacitors, $2(m-1)$ switching devices, $(m-1)(m-2)$ clamping diodes for a 'm' level DC-DC boost converter and it operates with high voltage gain without using transformers. The Switching of those power switches are controlled by Fuzzy logic controllers and they are made to operate in zero voltage switching mode (ZVS). Therefore, the proposed converter cannot only operate with high voltage gain, but also makes the duty cycles of power switches closer to 0.4. Moreover voltage across the capacitors in series is well balanced in both steady and dynamic states.

I. INTRODUCTION

Photovoltaic systems are expected to play an important role in future energy production. Such photovoltaic system consists of a solar module, a high step-up converter, a charge-discharge controller, a battery set, and an inverter. The step-up converter performs importantly among the system because the system requires a sufficiently high step-up conversion. This project mainly deals with step up converters used in photovoltaic generation system. Generally the photovoltaic systems can able to generate low output voltage. In order to connect the Photovoltaic system to the grid the voltage level should be adjusted according to the electrical network standards in the countries. First of all the voltage should be stepped up to sufficient level at which the DC/AC conversion can be performed to AC mains voltage requirements. Overall performance of the renewable energy system is then affected by the efficiency of step-up DC/DC converters.

High gain DC/DC converters are the key part of renewable energy systems. The designing of high gain DC/DC converters is imposed by severe demands. Designers face contradictory constraints such as low cost and high reliability. The main problem for the operator is to maximize the energy yield and to minimize the maintenance. For these reasons the converters must be distinguished by high efficiency over wide input power and voltage range. High voltage gain is required to produce sufficient DC bus voltage level. Additionally they should operate at wide temperature range expressing low EMC emission and be immune to environmental conditions. Such demands create severe constraints for DC/DC boost converter designing which are key parts in terms of efficiency of overall renewable energy systems.

High efficiency of step-up DC/DC converters can be achieved by decreasing duty cycle (lower conduction losses) and reducing voltage stress on switches (cheaper and lower RDS-on switches) applying soft switching technique (minimizing switching losses) and utilizing active clamp circuits (recycling the energy stored in parasitic inductances). The proposed topology is established without a transformer or coupled inductors into account. It is composed of only one inductor, two output capacitors in series, and other power semiconductor components, which are easy to be integrated.

This proposed converter cannot only realize high step-up gain, but also avoid extreme duty cycles. In Section II, the deduction of the topology synthesis of the hybrid boost three-level dc-dc converter is clarified with the basic topological constraints of PulseWidth Modulation (PWM) converters, based on the topology synthesis technique. The converter’s principle of high voltage gain and non-extreme duty cycle’s operation is explained in the following Section. Finally, a 1-kw prototype is set up, and the effective experimental results are obtained.

II. OPERATION OF MULTILEVEL CONVERTER

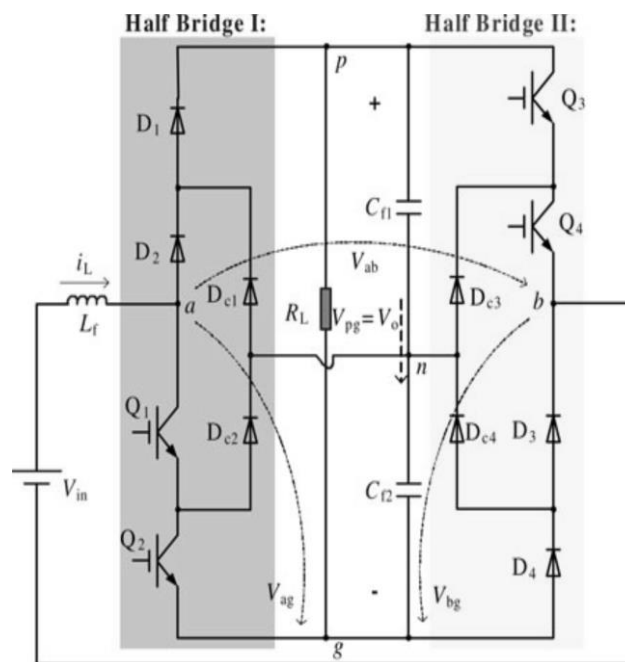


Fig.1. Proposed multilevel DC-DC converter

Table.1 SWITCHING STATES OF POWER SWITCHES

V_{ag}	V_{bg}	V_{ab}	Q_1-Q_2
$V_{cf1}+V_{cf2}$	0	V_o	0000
$V_{cf1}+V_{cf2}$	V_{cf2}	$V_o/2$	0001
V_{cf2}	0	$V_o/2$	1000
0	0	0	1100
V_{cf2}	V_{cf2}	0	1001
$V_{cf1}+V_{cf2}$	$V_{cf1}+V_{cf2}$	0	0011

The output pulse voltages of two half bridges are V_{ag} and V_{bg} , and then the output pulse voltage V_{ab} of the hybrid converter can be described as $V_{ab} = V_{ag} - V_{bg}$. As a result, the output dc voltage $V_{pg} = V_o$ can be obtained from V_{ab} , filtering by capacitors C_{f1} and C_{f2} . The corresponding states of power components for instantaneous V_{ab} of the hybrid converter are listed below, and it is also assumed that the voltages across capacitors C_{f1} and C_{f2} are equal, namely $V_{Cf1} = V_{Cf2}$. When the power switches $Q_1 - Q_4$ are turned OFF, the capacitors C_{f1} and C_{f2} in series are charged together by both the dc voltage source V_{in} and the energy stored in L_f through diodes $D_1 - D_4$.

Then, the instantaneous V_{ab} of the hybrid converter is V_o . While C_{f1} is charged by V_{in} , as well as the energy stored in L_f through diodes D_2, D_1 , and D_{c3} when only Q_4 is turned ON. At the same time, C_{f2} is discharged for the load, and the instantaneous V_{ab} is $V_o/2$, which is the voltage across C_{f1} . In addition, the redundant state for the instantaneous $V_{ab} = V_o/2$ is that C_{f2} is charged by V_{in} and the energy stored in L_f through diodes D_{c2}, D_4 , and D_3 when only Q_1 is turned ON. Meanwhile, C_{f1} is discharged for the load, and V_{ab} is the voltage across C_{f2} . When the power switches Q_1 and Q_2 are turned ON, the energy is stored in L_f through diodes D_4 and D_3 , while C_{f1} and C_{f2} are discharged together for the load. Then, the instantaneous V_{ab} is zero. Moreover, the other two redundant states for $V_{ab} = 0$ is that power switch pairs (Q_1, Q_4) , or (Q_3, Q_4) are turned ON, respectively, the energy is stored in L_f by V_{in} through the corresponding diodes, while C_{f1} and C_{f2} are discharged together for the load.

PWM CONTROL

The switching functions of V_{ag} and V_{bg} for both half-bridges can be described as follows:

$$V_{ag} = (1 - S_1 \cdot S_2) \cdot (V_{Cf1} + V_{Cf2}) - (S_1 - S_2) \cdot V_{Cf1}$$

$$V_{bg} = S_3 \cdot V_{Cf1} + S_4 \cdot V_{Cf2}$$

Where S_x ($x = 1, 2, 3, 4$) = "0" or "1" is the function of the switching state of the corresponding power switch.

According to (1) - (3), the switching function of V_{ab} for the hybrid converter can be written as

$$V_{ab} = [(1 - S_1) \cdot (1 + S_2) - S_3] \cdot V_{Cf1} + (1 - S_1 \cdot S_2 - S_4) \cdot V_{Cf2}$$

Then, the PWM control method can be depicted in figure, according to above equations and the consideration that switching actions are the least between two adjacent switching states $(S_1 S_2 S_3 S_4)$ in one carrier period, as well as the required balancing principle for charging or discharging of C_{f1} and C_{f2} . In Fig, m_a and m_b are the modulation indexes for the double modulation waves, and carrier_1, carrier_2 are designed as π phase-shifted carriers due to the two half bridges structure of the hybrid converter. In addition, the PWM control law can be described as

$$m_b > V_{carrier-1}, S_1 = 0$$

$$m_a > V_{carrier-2}, S_2 = 1$$

$$m_a > V_{carrier-1}, S_3 = 1$$

$$m_b > V_{carrier-2}, S_4 = 0$$

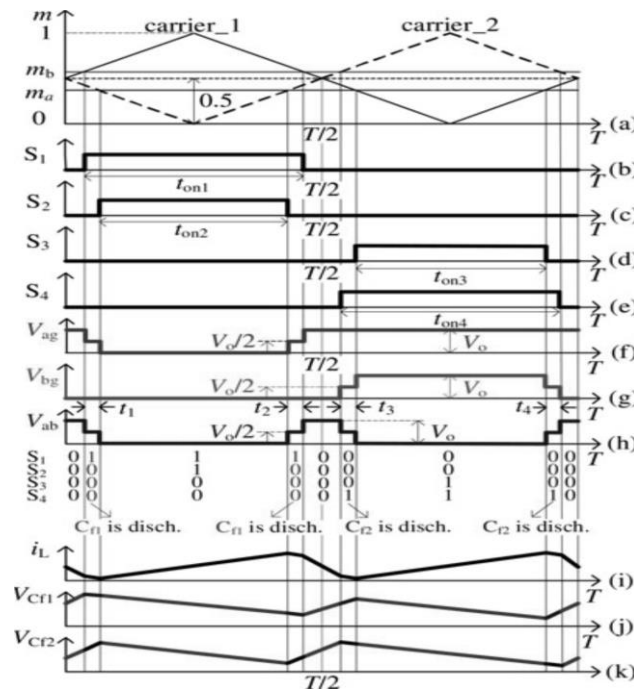


Fig.2. PWM control method

OPERATION WITH HIGH VOLTAGE GAIN

According to the operation states of the multilevel converter, energy W_{st} is stored in L_f when $V_{ab} = 0$, otherwise, energy W_{tr} is transferred. It is assumed that the inductor current i_L is continuous, and I_L is its average current. Then, W_{st} and W_{tr} can be described in one carrier period as follows:

$$W_{st} = V_{in} \cdot I_L \cdot t_{on} * 2$$

$$W_{tr} = (V_o - V_{in}) \cdot I_L \cdot (T/2 - t_{on1}) * 2 + (V_o/2 - V_{in}) \cdot I_L \cdot (t_1 + t_2) * 2$$

$$W_{st} = W_{tr}$$

The output voltage is given as

$$V_o = V_{in} \cdot \frac{T}{T - (t_{on1} + t_{on2})} = \frac{V_{in}}{1 - (d_1 + d_2)}$$

Where d_1 and d_2 are the duty cycles of Q_1 and Q_2 , respectively.

Then, all the duty cycles of power switches can be described as follows with the modulation indexes m_a and m_b .

$$d_1 = d_4 = 1 - m_b$$

$$d_2 = d_3 = m_a$$

Where d_3 and d_4 are the duty cycles of Q_3 and Q_4 , respectively.

Then, the voltage gain M of the proposed converter is written as follows

$$M = \frac{V_o}{V_{in}} = \frac{1}{1 - (d_1 + d_2)} = \frac{1}{m_b - m_a}$$

In terms of above equation, it can be concluded that the closer m_b and m_a get, the higher the voltage gain is. Moreover, the extreme duty cycles of the power switches can be avoided, if both m_b and m_a are around 0.4 with the limited conditions: $m_a < 0.4 < m_b$, and $m_b + m_a < 1$. As to the given voltage gain M , there is an infinite number of solutions to m_b and m_a . However, a tradeoff between the non-extreme duty cycles of power switches and the fluctuating amplitude of the inductor current must be well considered, and the better solution in this letter is described as

$$m_b = 0.5 + 1/4M$$

$$m_a = 0.5 - 1/4M$$

The blocking voltages across Q_1 , Q_2 and the inductor current in steady state are shown in Fig. 4.2, when the load resistor R_L is 360 Ω . It is shown that the blocking voltages of Q_1 and Q_2 are half of the output dc voltage (300 V), and the duty cycles d_1 and d_2 are about 48% and 44% respectively, rather than 91.7% (11/12) when the voltage gain is $M = 12$. In addition, the fluctuating amplitude of i_L is about 6.4 A (i_L is measured by Current Sensor-CSM050AP). The output three-level voltages V_{ag} and V_{bg} of both half-bridges are shown in Fig. 4.2, and the output three-level voltage V_{ab} (narrow pulse voltage) of the hybrid converter is obtained by the difference between V_{ag} and V_{bg} .

In order to verify the converter's performance for the step change of the load, the voltages across C_1 , C_2 and the load, as well as the inductor current, are shown in Fig. 4.2 with the load resistor step change from 720 to 360 Ω . The capacitor voltages V_{Cf1} and V_{Cf2} , both are stabilized at 300V before the load step change, and V_o is naturally controlled at 300 V stably. While i_L fluctuates from 7.9 to 14.5 A. After the load step change, both capacitor voltages are stabilized at 300 V again with the adjustment time about 16 ms, namely, the capacitor voltages can be balanced, though it is under load step change condition. In addition, the inductor current increases and adjusts, and then it fluctuates from 20 to 26.4 A in the steady state.

Table.2 EXPERIMENTAL PARAMETERS AND COMPONENTS

S.NO	COMPONENTS	VALUES (Units)
1	DC Input voltage V_{in}	50V
2	Output voltage V_{ref}	300V
3	Inductor L_f	317 μ H
4	Output filtering capacitors $C_{f1}=C_{f2}$	100 μ F
5	Load resistor R_L	300-2000 Ω
6	Switching frequency f_c	12.5 kHz
7	Power switches Q_1 - Q_4	FGA30N60 (600V, 30A)
8	Diodes D_1 - D_4 and D_{c1} - D_{c4}	MUR3060 (600V, 30A)
9	Rated power P_n	1 kW

Therefore, the proposed converter is suitable for the high step-up dc-dc voltage source interface of PV generation systems.

III. EXPERIMENT RESULTS

The experimental parameters and components are listed in Table II, and the FUZZY LOGIC Controller of voltage loop, which is not discussed in this paper, is adopted to control the output dc voltage. It is clear that the blocking voltages of Q_1 and Q_2 are half of the output dc voltage (600V), and the duty cycles d_1 and d_2 are about 48% and 44% respectively, rather than 91.7% (11/12) when the voltage gain is $M = 12$. In addition, the fluctuating amplitude of i_L is about 6.4 A (i_L is measured by Current Sensor-CSM050AP). The output three-level voltages V_{ag} and V_{bg} of both half-bridges and the output three-level voltage V_{ab} (narrow pulse voltage) of the multilevel converter is obtained by the difference between V_{ag} and V_{bg} . The capacitor voltages V_{Cf1} and V_{Cf2} , both are stabilized at 300 V before the load step change, and V_o is naturally controlled at 600 V stably. While i_L fluctuates from 7.9 to 14.5 A. After the load step change, both capacitor voltages are stabilized at 300 V again with the adjustment time about 16 ms, namely, the capacitor voltages can be balanced, though it is under load step change condition. In addition, the inductor current increases and adjusts, and then it fluctuates from 20 to 26.4 A in the steady state.

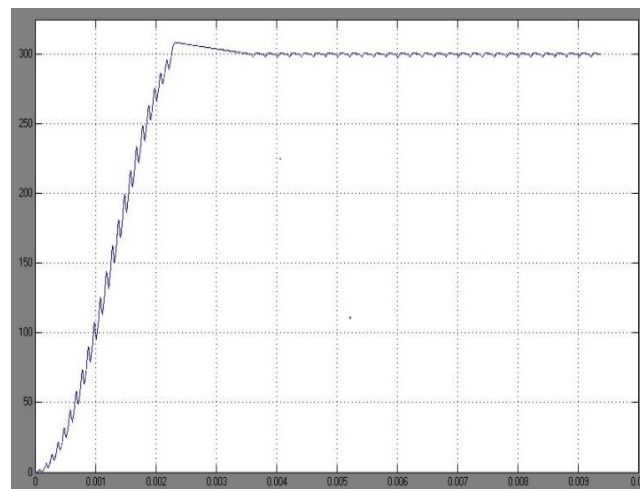


Fig.3. Output voltage of Multilevel converter

IV. CONCLUSION

The multilevel DC-DC boost converter with ZVS topology is presented and performance is analyzed. This proposed converter topology is made to operate at ZVS mode so the voltage stress on switches and switching power loss is reduced. It cannot only operate with transformer less high voltage gain, but also make the duty cycles of the power switches closer to 0.4 with the increasing voltage gain, instead of the extreme duty cycles. Moreover the capacitor voltages can be balanced both in dynamic and steady states by the proposed PWM control method with the help of Fuzzy logic controller. Therefore the proposed converter is suitable for PV generation systems connected to the grid with the parallel connected low-voltage PV arrays.

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